In the Claims:

1. (Canceled)

2. (Currently Amended) The method according to Claim 28, further comprising chemically-mechanically polishing (CMP) the surface of the workpiece ~~wafer~~ to remove the first conductive layer, second conductive material, thin dielectric layer, and third conductive material from the top surface of the insulating layer, to form ~~leaving~~ at least one vertical MIMCap in the MIMCap region of the insulating layer ~~first region~~.

3. (Currently Amended) The method according to Claim 2, wherein a plurality of vertical MIMCap's are formed in the MIMCap region of the insulating layer ~~first region~~, further comprising coupling at least two of the vertical MIMCap's together.

4. (Currently Amended) The method according to Claim 2, wherein the CMP simultaneously forms MIMCap's in the MIMCap region of the insulating layer ~~material first region~~ and conductive wiring in the wiring region of the insulating layer ~~material second region~~.

5. (Previously Presented) The method according to Claim 28, wherein depositing the first conductive layer comprises depositing a conductive liner.

6. (Original) The method according to Claim 5, wherein depositing the first conductive layer comprises forming a conductive seed layer over the conductive liner.

7. (Original) The method according to Claim 6, wherein the conductive liner and conductive seed layer comprise at least one MIMCap bottom plate.

8. (Currently Amended) The method according to Claim 6, wherein depositing the conductive liner comprises depositing TaN, Ta, TiN or combinations thereof by chemical vapor deposition (CVD) or physical conductive vapor deposition (PVD), and wherein forming the conductive seed layer comprises depositing a copper seed layer by PVD or CVD.

9. (Currently Amended) The method according to Claim 28, wherein depositing the second conductive material ~~layer~~ comprises depositing copper by electroplating or physical vapor deposition (PVD), wherein depositing the third conductive material comprises depositing W, TiN, Al, Ta, Ti, TaN, TiW, Cu, Si, or combinations thereof by physical vapor deposition (PVD) or chemical vapor deposition (CVD), and wherein the third conductive material forms the MIMCap top plate.

10. (Previously Presented) The method according to Claim 28, wherein depositing the thin dielectric layer comprises depositing a conformal dielectric having a thickness of 10 nm to 200 nm.

11. (Original) The method according to Claim 10, wherein depositing the thin dielectric layer comprises depositing silicon nitride, $Ta_2O_5$, or combinations thereof by plasma-enhanced chemical vapor deposition (PECVD).

12. (Currently Amended) A method of fabricating a vertical metal-insulator-metal capacitor (MIMCap), comprising:

providing a workpiece;

depositing an inter-level dielectric over the workpiece;

patterning the inter-level dielectric to form a plurality of trenches having ~~, said inter-level dielectric comprising at least one first region and at least one second region, the first region comprising trenches for at least one MIMCap, the second region comprising trenches for a plurality of conductive lines, wherein the trenches in the first region and the trenches in the second region have~~ substantially vertical sidewalls and equal height and width dimensions;

defining a first region of said inter-level dielectric comprising first trenches of said plurality of trenches for at least one MIMCap and defining a second region of said inter-level dielectric comprising second trenches of said plurality of trenches for a plurality of conductive lines;

depositing a conductive liner over the inter-level dielectric and within the trenches of said first and second regions;

depositing a seed layer over the conductive liner;

depositing a resist over the seed layer;

selectively removing the resist over the seed layer in the inter-level dielectric second region and ~~regions,~~ leaving resist over the seed layer in the inter-level dielectric first regions;

depositing a first conductive material within the inter-level dielectric second region trenches to overfill the trenches and to form said plurality ~~a plurality~~ of conductive lines;

removing the resist covering the first region;

depositing a MIMCap dielectric over the first conductive material within the second region trenches and over the first conductive layer within the first region trenches; and

depositing a second conductive material over the MIMCap dielectric within the first region trenches to form a MIMCap top plate, wherein the second conductive material overfills ~~completely fills~~ the first region trenches.

13. (Currently Amended) The method according to Claim 12, further comprising chemically-mechanically polishing (CMP) the workpiece ~~the top surface of the wafer~~ to remove the conductive liner, seed layer, first conductive material, MIMCap dielectric, and second conductive material from the top surface of the inter-level dielectric, to form ~~leaving~~ at least one vertical MIMCap in the ~~insulating layer~~ first region of said inter-level dielectric.

14. (Currently Amended) The method according to Claim 13, wherein a plurality of vertical MIMCap's are formed in said first region of the inter-level dielectric ~~first region~~, further comprising coupling at least two of the vertical MIMCap's together.

15. (Currently Amended) The method according to Claim 13, wherein the CMP simultaneously forms at least one MIMCap in the first region of the inter-level dielectric ~~first region~~ and the plurality of conductive lines in the second region of the inter-level dielectric ~~second region~~.

16. (Original) The method according to Claim 12, wherein the conductive liner and conductive seed layer comprise at least one MIMCap bottom plate.

17. (Original) The method according to Claim 12, wherein depositing the conductive liner comprises depositing TaN, Ta, TiN or combinations thereof by chemical vapor deposition (CVD) or physical conductive vapor deposition (PVD), wherein forming the conductive seed layer comprises depositing a copper seed layer by PVD or CVD.

18. (Currently Amended) The method according to Claim 12, wherein depositing the first conductive material ~~layer~~ comprises depositing copper by electroplating or physical vapor deposition (PVD), wherein depositing the second conductive material comprises depositing W, TiN, Al, Ta, Ti, TaN, TiW, Cu, Si, or combinations thereof by physical vapor deposition (PVD) or chemical vapor deposition (CVD).

19. (Original) The method according to Claim 12, wherein depositing the MIMCap dielectric comprises depositing a conformal dielectric having a thickness of approximately 10 nm to 200 nm.

20. (Original) The method according to Claim 19, wherein depositing the MIMCap dielectric comprises depositing silicon nitride, $Ta_2O_5$, or combinations thereof by plasma-enhanced chemical vapor deposition (PECVD).

21-27 (Canceled)

28. (Currently Amended) A method of fabricating a metal-insulator-metal capacitor (MIMCap), comprising:

depositing an insulating layer over a workpiece~~, the insulating layer including a MIMCap region and wiring region~~;

forming ~~patterning the insulating layer to form~~ a plurality of trenches, each trench of said plurality including a bottom and substantially vertical sidewalls and each trench ~~in the MIMCap region~~ having substantially equal height and width dimensions ~~as each trench in the wiring region~~;

depositing a first conductive layer over the insulating layer and over the bottom and sidewalls of each trench of said plurality of ~~within the~~ trenches ~~in both the MIMCap region and the wiring region~~;

defining a region of said insulating layer having at least one trench of said plurality of trenches as a MIMCap region and defining another region of said insulating layer having other trenches of said plurality of trenches as a wiring region;

forming ~~depositing~~ a resist over the MIMCap region of the insulating layer and leaving the wiring region uncovered;

depositing a second conductive material over the uncovered ~~within the trenches in the~~ wiring region of the insulating layer such that said second conductive material overfills the trenches in the wiring region;

removing the resist from the MIMCap region to expose trenches in the MIMCap region;

depositing a thin dielectric layer over the second conductive material covering ~~within~~ the wiring region including the overfilled trenches and over the exposed first conductive layer within the MIMCap region trenches; and

depositing a third conductive material over the thin dielectric layer within the MIMCap region trenches such that ~~to completely fill~~ the MIMCap region trenches are overfilled.